Area Array Interconnection Handbook

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Microelectronic packaging has been recognized as an important "enabler" for the solid state revolution in electronics which we have witnessed in the last third of the twentieth century. Packaging has provided the necessary external wiring and interconnection capability for transistors and integrated circuits while they have gone through their own spectacular revolution from discrete device to gigascale integration. At IBM we are proud to have created the initial, simple concept of flip chip with solder bump connections at a time when a better way was needed to boost the reliability and improve the manufacturability of semiconductors. The basic design which was chosen for SLT (Solid Logic Technology) in the 1960s was easily extended to integrated circuits in the '70s and VLSI in the '80s and '90s. Three I/O bumps have grown to 3000 with even more anticipated for the future. The package families have evolved from thick-film (SLT) to thin-film (metallized ceramic) to co-fired multi-layer ceramic. A later family or ceramics with matching expansivity to sili con and copper internal wiring was developed as a predecessor of the chip interconnection revolution in copper, multilevel, submicron wiring. Powerful server packages have been de veloped in which the combined chip and package copper wiring exceeds a kilometer. All of this was achieved with the constant objective of minimizing circuit delays through short, efficient interconnects.

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